

WHAT IS CLAIMED IS:

1 1. A circuit for providing generalized write pre-compensation, comprising:
2 a coarse phase generator for generating N coarse phase signals;
3 a fine phase generator, coupled to the coarse phase generator, for using the N
4 coarse phase signals to generate M fine phase signals; and
5 a write pre-compensation circuit, coupled to the fine phase generator, for
6 choosing a fine phase signal from the M fine phase signals to provide a shift to received
7 write data to achieve a first desired pre-compensation.

1 2. The circuit of claim 1, wherein the fine phase signal chosen provides a
2 shift to received write data to achieve a first desired positive pre-compensation.

1 3. The circuit of claim 1, wherein the fine phase signal chosen provides a
2 shift to received write data to achieve a first desired negative pre-compensation.

1 4. The circuit of claim 1, wherein the fine phase signal is chosen to further
2 provide a shift to received write data to achieve positive or negative timing asymmetry
3 correction.

1 5. The circuit of claim 1, wherein the coarse phase generator comprises a X
2 stage differential ring VCO running at a first frequency and providing 2X phase signals
3 of 0° to 360° in 360°/(2X) increments.

1 6. The circuit of claim 1, wherein the coarse phase generator comprises a X
2 stage differential ring VCO running at a second frequency, the coarse phase generator
3 further comprises differential dividers and provides 4X phase signals of 0° to 360° in
4 360°/(8X) increments.

1 7. The circuit of claim 1, wherein the fine phase generator comprises an
2 interpolator for providing voltage averaging to generate the M fine phase signals.

1 8. The circuit of claim 7, wherein the fine phase generator further comprises
2 drivers receiving one of the N coarse phase signals and serially coupled resistors disposed
3 between the drivers for generating the M fine phase signals.

1 9. The circuit of claim 1, wherein the write pre-compensation circuit further
2 comprises:
3 a pre-compensation decoder, coupled to the fine phase generator, the pre-
4 compensation decoder receiving a reference clock from the fine phase generator, the pre-
5 compensation decoder receiving the write data;
6 a latch circuit, coupled to the fine phase generator and the pre-compensation
7 decoder, the latch circuit being supplied the write data from the pre-compensation
8 decoder and the M fine phase clock signals, the latch circuit supplying M latched write
9 data signals shifted according to the M fine phase clock signals; and
10 a data selector, coupled to the latch circuit and the pre-compensation decoder, the
11 data selector receiving a data selection signal from the pre-compensation decoder for
12 indicating to the data selector which of the shifted M latched write data signals to provide
13 as pre-compensated write data.

1 10. The circuit of claim 9 further comprises a write driver, the write driver
2 receiving the pre-compensated write data and outputting NRZI write data.

1 11. The circuit of claim 10, wherein a shifted M latched write data signal is
2 chosen to further provide a shift to received write data to achieve timing asymmetry
3 correction.

1 12. The circuit of claim 9 further comprising a divider for dividing the
2 reference clock to increase a slew rate of the M fine phase clock signals and to provide a
3 wider frequency range for the M fine phase clock signals, the coarse phase clock signals
4 used is changed to provide the first desired pre-compensation.

1 13. A magnetic storage device, comprising:
2 a magnetic storage medium for recording data thereon;
3 a motor for moving the magnetic storage medium;
4 a head for reading and writing data on the magnetic storage medium;
5 an actuator for positioning the head relative to the magnetic storage medium; and
6 a data channel for processing encoded signals on the magnetic storage medium,
7 the data channel comprising a coarse phase generator for generating N coarse phase
8 signals, a fine phase generator, coupled to the coarse phase generator, for using the N
9 coarse phase signals to generate M fine phase signals and a write pre-compensation
10 circuit, coupled to the fine phase generator, for choosing a fine phase signal from the M
11 fine phase signals to provide a shift to received write data to achieve a first desired pre-
12 compensation.

1 14. The magnetic storage device of claim 13, wherein the fine phase signal
2 chosen provides a shift to received write data to achieve a first desired positive pre-
3 compensation positive pre-compensation.

1 15. The magnetic storage device of claim 13, wherein the fine phase signal
2 chosen provides a shift to received write data to achieve a first desired negative pre-
3 compensation positive pre-compensation.

1 16. The magnetic storage device of claim 13, wherein the fine phase signal is
2 chosen to further provide a shift to received write data to achieve timing asymmetry
3 correction.

1 17. The magnetic storage device of claim 13, wherein the coarse phase
2 generator comprises a X stage differential ring VCO running at a first frequency and
3 providing 2X phase signals of 0° to 360° in $360^\circ/(2X)$ increments.

1 18. The magnetic storage device of claim 13, wherein the coarse phase
2 generator comprises a X stage differential ring VCO running at a second frequency, the
3 coarse phase generator further comprises differential dividers and provides 4X phase
4 signals of 0° to 360° in $360^\circ/(8X)$ increments.

1 19. The magnetic storage device of claim 13, wherein the fine phase generator
2 comprises an interpolator for providing voltage averaging to generate the M fine phase
3 signals.

1 20. The magnetic storage device of claim 19, wherein the fine phase generator
2 further comprises drivers receiving one of the N coarse phase signals and serially coupled
3 resistors disposed between the drivers for generating the M fine phase signals.

1 21. The magnetic storage device of claim 13, wherein the write pre-
2 compensation circuit further comprises:
3 a pre-compensation decoder, coupled to the fine phase generator, the pre-
4 compensation decoder receiving a reference clock from the fine phase generator, the pre-
5 compensation decoder receiving the write data;
6 a latch circuit, coupled to the fine phase generator and the pre-compensation
7 decoder, the latch circuit being supplied the write data from the pre-compensation
8 decoder and the M fine phase clock signals, the latch circuit supplying M latched write
9 data signals shifted according to the M fine phase clock signals; and
10 a data selector, coupled to the latch circuit and the pre-compensation decoder, the
11 data selector receiving a data selection signal from the pre-compensation decoder for
12 indicating to the data selector which of the shifted M latched write data signals to provide
13 as pre-compensated write data.

1 22. The magnetic storage device of claim 21 further comprises a write driver,
2 the write driver receiving the pre-compensated write data and outputting NRZI write
3 data.

1 23. The magnetic storage device of claim 22, wherein a shifted M latched
2 write data signal is chosen to further provide a shift to received write data to achieve
3 timing asymmetry correction.

1 24. The magnetic storage device of claim 21 further comprising a divider for
2 dividing the reference clock to increase a slew rate of the M fine phase clock signals and
3 to provide a wider frequency range for the M fine phase clock signals, the coarse phase
4 clock signals used is changed to provide the first desired pre-compensation.

1 25. A method for providing generalized write pre-compensation, comprising:
2 generating N coarse phase signals;
3 using the N coarse phase signals to generate M fine phase signals; and
4 choosing a fine phase signal from the M fine phase signals to provide a shift to
5 received write data to achieve a first desired pre-compensation.

1 26. The method of claim 25, wherein the choosing a fine phase signal further
2 comprises choosing a fine phase signal to achieve a first desired positive pre-
3 compensation.

1 27. The method of claim 25, wherein the choosing a fine phase signal further
2 comprises choosing a fine phase signal to achieve a first desired negative pre-
3 compensation.

1 28. The method of claim 25, wherein the choosing a fine phase signal further
2 comprises choosing a fine phase signal to further provide a shift to received write data to
3 achieve positive or negative timing asymmetry correction.

1 29. The method of claim 25, wherein the generating N coarse phase signals
2 further comprises providing X phase signals of 0° to 360° in $360^\circ/X$ increments.

1 30. The method of claim 25, wherein the generating N coarse phase signals
2 further comprises providing 2X phase signals of 0° to 360° in 360°/(2X) increments.

1 31. The method of claim 25, wherein the using the N coarse phase signals to
2 generate M fine phase signals further comprises providing voltage averaging to the N
3 coarse phase signals to generate the M fine phase signals.

1 32. The method of claim 25, wherein the choosing a fine phase signal from the
2 M fine phase signals to provide a shift to received write data to achieve a first desired
3 pre-compensation further comprises:
4 shifting write data according to the M fine phase clock signals to produce M
5 shifted write data signals; and
6 in response to receiving a reference clock and write data, supplying a data
7 selection signal to choose one of the M shifted write data signals to provide as pre-
8 compensated write data.

1 33. The method of claim 32, wherein the supplying a data selection signal to
2 choose one of the M shifted write data signals to further achieve timing asymmetry
3 correction for the write data.

1 34. The method of claim 32 further comprising:
2 dividing the reference clock to increase a slew rate of the M fine phase clock
3 signals and to provide a wider frequency range for the M fine phase clock signals; and
4 changing the coarse phase clock signals used to provide the first desired pre-
5 compensation.